The listing of Claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Original) A fuse box of an integrated circuit device, comprising:

a fuse line at a fuse portion of the integrated circuit device;

a first insulating layer on the fuse line;

a first guard ring pattern that encloses the fuse line on the first insulating layer;

a second insulating layer on the first guard ring pattern and the first insulating layer;

a second guard ring pattern that encloses the fuse line on the second insulating layer; and

a passivation layer on the second insulating layer and the second guard ring pattern, the passivation layer defining at least a portion of a fuse opening having a sidewall in the first and second insulating layers and the passivation layer extending on the sidewall of the fuse opening to at least the first insulating layer.

2. (Withdrawn) The fuse box of Claim 1, further comprising:

a first fuse contact hole in the first insulating layer that encloses the fuse line;

a first fuse contact plug in the first fuse contact hole, wherein the first guard ring pattern is disposed on the first fuse contact plug and the first insulating layer;

a second fuse contact hole in the second insulating layer that encloses the fuse line; and

a second fuse contact plug in the second fuse contact hole, wherein the second guard ring pattern is disposed on the second fuse contact plug.

3. (Withdrawn) The fuse box of Claim 2, wherein the passivation layer extends on a surface of the second guard ring pattern, on a sidewall of the second insulating layer and on an exposed surface of the first insulating layer.

4. (Withdrawn) The fuse box of Claim 3, further comprising an etch stop layer between the fuse line and the first insulating layer and wherein the fuse opening extends through the etch stop layer.

5. (Withdrawn) The fuse box of Claim 1, wherein the first guard ring pattern comprises a first metal layer on the first contact plug and the first insulating layer and a first metal compound layer on the metal layer and wherein the second guard ring pattern comprises a second metal layer on the second contact plug and the second insulating layer and a second compound metal layer on the second metal layer.

6. (Original) The fuse box of Claim 1, further comprising:

a first fuse contact hole in the first insulating layer that encloses the fuse line;

a first fuse contact plug in the first fuse contact hole, wherein the first guard ring pattern is disposed on the first fuse contact plug and the first insulating layer and wherein the second guard ring pattern is disposed on a surface of the first guard ring pattern.

7. (Original) The fuse box of Claim 6, wherein the passivation layer is disposed on a surface of the second insulating layer, on a surface and a sidewall of the second guard ring pattern and an exposed surface of the first insulating layer.

8. (Original) The fuse box according to Claim 7, further comprising an etch stop layer between the fuse line and the first insulating layer, wherein the fuse opening extends through the etch stop layer.

9. (Original) A fuse box of an integrated circuit device comprising:

an insulation layer covering a fuse portion formed on an integrated circuit substrate;

a first interlayer dielectric having a metal plug enclosing the fuse portion;

a lower guard ring pattern enclosing the fuse portion, the lower guard ring pattern being formed on the metal plug and on the first interlayer dielectric adjacent to the metal plug;

a second interlayer dielectric having an opening partially exposing the fuse portion and the lower guard ring pattern; and

an upper guard ring pattern successively formed from the second interlayer dielectric adjacent to sidewalls of the opening and sidewalls of the metal plug.

10. (Original) The fuse box of an integrated circuit device according to Claim 9, further comprising an etch stop film pattern formed on the insulation layer to enclose the fuse portion, and wherein the metal plug is positioned on the etch stop film pattern.

11. (Original) The fuse box of an integrated circuit device according to Claim 9, wherein a groove prolonged from an inside of the metal plug is formed in the first interlayer dielectric by partially etching a portion of the first interlayer dielectric enclosed by the metal plug.

12. (Original) The fuse box of an integrated circuit device according to Claim 11, wherein the lower guard ring pattern comprises a first metal layer pattern and a first metal compound layer pattern formed on the first metal layer pattern.

13. (Original) The fuse box of an integrated circuit device according to Claim 12, wherein the first metal layer pattern comprises aluminum, and the first metal compound layer pattern comprises titanium nitride.

14. (Original) The fuse box of an integrated circuit device according to Claim 9, wherein the metal plug comprises tungsten.

15. (Original) The fuse box of an integrated circuit device according to Claim 9, wherein the first interlayer dielectric and the second interlayer dielectric comprise borophosphosilicate glass (BPSG).

16. (Original) An integrated circuit device comprising:

a fuse portion where a fuse line is formed on an integrated circuit substrate;

an insulation film covering the fuse line;

a polysilicon pattern formed on the insulation film to enclose the fuse portion;

a first interlayer dielectric formed on the polysilicon pattern, the first interlayer dielectric having a fuse contact hole enclosing the fuse portion and partially exposing the polysilicon pattern;

a metal plug filling up the fuse contact hole;

a lower guard ring pattern enclosing the fuse portion, the lower guard ring pattern being formed on the metal plug and the first interlayer dielectric adjacent to the metal plug;

a second interlayer dielectric having an opening partially exposing the fuse portion and a portion of the lower guard ring pattern;

an upper guard ring pattern successively formed from the second interlayer dielectric to sidewalls of the opening and sidewalls of the metal plug; and

a passivation layer formed on the second interlayer dielectric to cover the upper guard ring pattern, the passivation layer having a fuse opening that exposes the insulation film.